Notice of Allowability	Application No.	Applicant(s)	
	10/718,563	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment and drawing correction filed 6/9/05*.

2. ☒ The allowed claim(s) is/are *2-9,11 and 17-20*.

3. ☒ The drawings filed on *09 June 2005 and 24 November 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Minhloan Tran
Primary Examiner
Art Unit 2826

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jason Vick on 6/17/05.

2. The application has been amended as follows:

IN THE CLAIMS:

(1) In claim 3, line 8, change "above a channel region" to

– above said channel region –

(2) In claim 3, line 11, change "above a channel region" to

– above said channel region –

REASONS FOR ALLOWANCE

3. The following is an examiner's statement of reasons for allowance:

Claims 2-9,11, and 17-20 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a nonvolatile semiconductor memory device, comprising a source region and a drain region that are positioned at a specified distance from each other; a main surface of a semiconductor substrate; a channel region that is

formed between said source region and said drain region; a first gate that is provided above said channel region on a side toward said drain and via a first gate dielectric film; a second gate that is provided above said channel region on a side toward said source via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film; wherein the source region and the drain region are mounted on the main surface of the semiconductor substrate; said first gate is formed so as to cover said first gate dielectric film, the lateral surface of said first dielectric film, and the lateral surface of said second dielectric film; one end of said first gate is positioned on an upper end face of said second dielectric film; and said first gate is positioned with both ends placed in a gap region enclosed by said second gate and is filled so as to form a concave portion, as recited in claim 2, or wherein the source region and the drain region are mounted on the main surface of the semiconductor substrate; said first gate is formed so as to cover said first gate dielectric film, the lateral surface of said first dielectric film, and the lateral surface of said second dielectric film; one end of said first gate is positioned on an upper end face of said second dielectric film; and the surface area of said first gate is A > B+C+D when the sidewall area within a gap region of said second gate is A, the bottom surface area within a gap region of said second gate is B, the flat surface area of the top of said second gate is C, and the sidewall area of the top of said second gate is D, as recited in claim 3, or wherein a first conductive well is formed on the main surface

of a semiconductor substrate so that the source region and the drain region are formed in said first conductive well; a third gate is provided via a third dielectric film formed on said first gate; and a bind region for binding a plurality of said second gates is provided on a region of said semiconductor substrate where an impurity diffusion layer including a second conductivity type is selectively formed; and an impurity diffusion layer region including said second conductivity type is connected to said source region, said drain region, and a diffusion layer region of a select transistor for selecting said source region and drain region, as recited in claim 11.

As was explained in the paper mailed 12/6/04, SHIN 6,476,440 discloses each and every limitation of claims 2 and 3 except that a first gate is positioned with both ends placed in a gap region enclosed by a second gate and is filled so as to form a concave portion, as recited in claim 2, and except that a surface area of said first gate is A > B+C+D when the sidewall area within a gap region of said second gate is A, the bottom surface area within a gap region of said second gate is B, the flat surface area of the top of said second gate is C, and the sidewall area of the top of said second gate is D, as recited in claim 3.

Further, SHIN in view of HARARI ET AL. 6,103,573, renders obvious all features of claim 11 except that an impurity diffusion layer region including said second conductivity type is connected to said source region, said drain region, and a diffusion layer region of a select transistor for selecting said source region and drain region.

With regard to claim 8, Kobayashi 2003/0103382 discloses a nonvolatile semiconductor memory device, comprising a source region 105 and a drain region (also numbered 105) that are positioned at a specified distance from each other and disposed on a main surface of a semiconductor substrate 100; a channel region (not marked in the figure) that is formed between said source region 105 and said drain region 105; a first gate 107b that is provided above said channel region on a side toward said drain region 105 via a first gate dielectric film 106a; a second gate 103a that is provided above said channel region on a side toward said source region 105 via a second gate dielectric film 102, wherein a lateral surface of said second gate 103a is covered with a first dielectric film 106b and an upper surface of said second gate 103a is provided with a second dielectric film 104b; a third gate 110a provided via a third dielectric film 109a formed on said first gate 107b; a word line (also numbered 110a) electrically connected to said third gate 110a; a contact hole (contact hole and metal wiring are not shown but are described at paragraph 0124) formed on said word line 110a; and metal wiring is connected to said word line 110a via said contact hole. Note figures 1 and 14 and paragraphs 106-131 of Kobayashi. However, Kobayashi does not disclose or suggest that said contact hole is provided above a member having the same material and film thickness as a film that forms said second gate 103a.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should pref-

erably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
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